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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,289	10/31/2003	Manolito M. Catalasan	1875.4360005	8425

28393 7590 09/02/2005

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,289	CATALASAN ET AL.	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 12-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,12-14,27 and 28* is/are rejected.

7)☒ Claim(s) *3-9, 15-26, 29, 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Or-Bach et al. (US 6,331,790).

3. With respect to claims 1 and 13, figures 1-70 of Or-Bach teach an integrated circuit chip including a plurality of metal layers (figure 15), first and second supply potentials (figure 56) and at least two adjacent logic blocks (201, 203), a modifiable circuit for coupling the at least two adjacent logic blocks (figure 3, I, II), comprising:

a first metal interconnect structure (3988, figure 56A) that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;

a second metal interconnect structure (3989, figure 56A) that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks;

an interconnect (figure 4 shows the logic block are connected together) formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect

structures, wherein a state of said interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers;

wherein said first metal interconnect structure (3988) is coupled to one of the first (VDD) and second supply potentials and the second metal interconnect structure (3989) is coupled to the other one of the first and second supply potentials (VSS).

4. With respect to claim 12, the apparatus of Or-Bach teaches reprogrammed by altering any one of the plurality of via layers and or metal layers.

5. Claims 1, 12-14, 27 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Bansal (US 6,765,245).

6. With respect to claims 1 and 13, figures 1-12 of Bansal teach an integrated circuit chip including a plurality of metal layers (column 3, lines 3-25), first and second supply potentials (5 and 6) and at least two adjacent logic blocks (figure 3), a modifiable circuit for coupling the at least two adjacent logic blocks (metal interconnects and vias), comprising:

a first metal interconnect structure (5) that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;

a second metal interconnect structure (6) that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks;

an interconnect (see figure 9, shows interconnect) formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect structures,

wherein a state of said interconnect is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers;

wherein said first metal interconnect structure (5) is coupled to one of the first (VDD) and second supply potentials and the second metal interconnect structure (6) is coupled to the other one of the first and second supply potentials (GND).

7. With respect to claim 12, the apparatus of Bansal teaches reprogrammed by altering any one of the plurality of via layers and or metal layers.

8. With respect to claim 13, the apparatus of Bansal discloses the first and second metal interconnection structures are not connected to each other at a top metal layer thereby forming two interconnects between the at least two adjacent logic blocks (see figure 9, 5 and 6 does not connect).

9. With respect to claim 14, the apparatus of Bansal teaches the first and second metal interconnect structures (M1 layer) is at a bottom metal layer (see column 6, lines 5-15).

10. With respect to claim 27, the apparatus of Bansal teaches an integrated circuit chip including a plurality of metal layers (M1-M5, see column 3, lines 2-25), first and second supply potentials and at least two adjacent logic blocks (see figure 9), a modifiable circuit for coupling the at least two adjacent logic blocks, comprising:

a first metal interconnect structure (5)that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;

a second metal interconnect structure (6) that traverses the plurality of metal layers

using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks; and

an interconnect formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect structures (see figure 9), wherein a state of said interconnect is programmable by altering any one of the plurality of metal layers and/or any one of a plurality of via layers;

wherein one of said first and second metal interconnect structures is coupled to the first supply potential (VDD, figure 9) at a bottom metal layer (M1) and the other of said first and second metal interconnect structures (6) is coupled to the second supply potential (GND) at the bottom metal layer, and

wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and/or any one of a plurality of via layers.

11. With respect to claim 28, the apparatus of Bansal teaches an integrated circuit chip including a plurality of metal layers, first and second supply potentials and at least two adjacent logic blocks, a modifiable circuit for coupling the at least two adjacent logic blocks, comprising:

a first metal interconnect structure (5) that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is located at a boundary of the at least two adjacent logic blocks;

a second metal interconnect structure (6) that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is located at said boundary of the at least two adjacent logic blocks; and

an interconnect formed between the at least two adjacent logic blocks by at least one of said first and second metal interconnect structures, wherein a state of said interconnect is programmable by altering any one of the plurality of metal layers and/or any one of a plurality of via layers (blocks are connected together using metal lines and vias);

wherein said first (5) and second (6) metal interconnect structures are not electrically coupled to each other at a top metal layer thereby forming two interconnects between the at least two adjacent logic blocks, and

wherein one of said first (5) and second (6) metal interconnect structures is coupled to the first supply potential (VDD) at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential (GND) at the bottom metal layer (M1).

Allowable Subject Matter

12. Claims 3-9, 15-26, 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is an examiner's statement of reasons for allowance:

With respect to claims 3 and 4, the prior art does not teach the first and second metal structures coupled together.

With respect to claims 15-17, 29 and 30, the prior art does not teach a ladder, or stacked structure.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

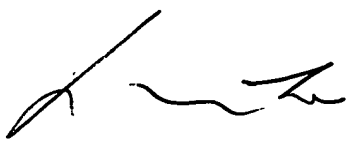
14. Applicant's arguments with respect to claims 1, 3-9 and 12-30 have been considered but are moot in view of the new ground(s) of rejection.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/31/2005



DON LE
PRIMARY EXAMINER